Amendments to the Specification

IN THE TITLE

On page 1, line 10, please capitalize the "p" of "phase" in the title.

Please delete the section entitled "Reference to Related Application" and replace the deleted section with the following replacement section:

REFERENCE TO RELATED APPLICATION

The present application is related to applicant's copending application entitled Data Aided Carrier Phase Timing Tracking System for Precoded Continuous Phase Modulated Signals, S/N: 09/694,650, filed 10/24/00, by the same inventors.

Please replace the paragraph beginning on page 13, line one and ending on page 14, line 9 with the following rewritten paragraph:

Referring to Figures 1A and 1B, and more particularly to the symbol time synchronizer of Figure 1B, a real component and an imaginary component of the r_n sampled input signal 14 are respectively isolated by an inphase component isolator 24 and a quadrature component isolator 26 respectively providing inphase and quadrature sample signals to an odd timing error detector 32 and an even timing error detector 34, that in turn, provide respective odd data and even data signals to a data demultiplexer 36 that provides the $\hat{d}_n$ estimated data sequence 15. The odd timing error detector 32

and even timing error detector 34 receive the inphase and quadrature sampled signals that are respectively communicated to early-late gates 44a and 44b and Laurent transformers $h_D(t)$ 46a and 46b isolating principal Laurent components. The Laurent transformer outputs of the transformers 46a and 46b are sampled by samplers 47a and 47b providing transformed sampled outputs. The early-late gate outputs of the early-late gates 44a and 44b are sampled by gate samplers 48a and 48b providing gate sampled outputs, respectively. The transformer sampled outputs of the transformer samplers 47a and 47b are respectively communicated to hard limiters 50a and 50b. The gate sampled outputs of the gate samplers 48a and 48b are respectively communicated to mixers 52a and 52b. The hard limiters 52a and 52b respectively provide the odd data and even data to the data ~~demultiplexer~~ multiplexer 36 that provides the $\hat{d}_n$ estimated data 15. The mixers 52a and 52b respectively mix odd and even data with the gate sampled outputs of gate samplers 48a and 48b to respectively provide e_{2k+1} odd and e_{2k} even timing signals that drive a loop filter 53, that in turn, controls a voltage controlled oscillator 54 used for generating the t_n timing signal. The e_{2k+1} odd and e_{2k} even timing signals are alternately processed and combined by the loop filter 53 for controlling the voltage controlled oscillator 54. The t_n timing signal 13 is further communicated to a modulo N counter 55 that provides the t_{mN} timing signals as well as generating the e_{2k+1} (2k+1)N odd and e_{2k} (2k)N even sampling signals that respectively control the samplers 47a and 47b, and, 48a and 48b. As may now be apparent, the synchronizer 10 operates in a timing loop extending through samplers 47ab, limiters 50ab, mixers 52ab, loop filter 53, VCO 54 and counter 55

for synchronized generation of the odd and even data and the t_n and t_{mN} timing signals, 13 and 17, respectively, while generating the $\hat{d}_n$ data estimates 15.

Please replace the paragraph beginning at page 15, line 4 and ending on page 16, line 11 with the following rewritten paragraph:

The carrier phase synchronizer 60 receives the t_n timing signal that may originate from the symbol time synchronizer 10 in the preferred form, or from a convention symbol timing tracking loop, not shown. The $r_n e^{-j\hat{\theta}}$ sample input signal 61 is communicated to an inphase component isolator 74 and a quadrature component isolator 76. The inphase component output of isolator 74 and the quadrature component output of isolator 76 are respectively sampled by an inphase sampler 80 and a quadrature sampler 82 at the rate of the t_n symbol timing signal 13 that also drives a modulo N counter 84 providing 2kN even and (2k+1)N odd timing sampling signals. The inphase sampler 80 provides a sampled inphase signal to an inphase transformer 86 as the quadrature sampler 82 provides a sampled quadrature signal to a quadrature transformer 88, providing respectively inphase and quadrature transformed signals to hard limiters 90a and 90b, and by cross coupling, to mixers 92b and 92a. The hard limiters 90a and 90b respectively provide inphase and quadrature hard limited signals to hard limiter samplers 94a and 94b that respectively sample at rates of the 2kN even and (2k+1)N odd timing sampling signals from the modulo N counter 84. The hard limiter samplers 94a and 94b respectively provide odd and even data

signals that are fed into a data ~~demultiplexer~~ multiplexer 94 for generating the $\hat{d}_n$ data estimate 15. The odd data and even data are respectively mixed with the quadrature and inphase transformed signals from the transformers 88 and 86, respectively, by the mixer 92a and 92b, for generating e_{2k+1} odd and $-e_{2k}$ even timing error signals. The $-e_{2k}$ timing error signal is inverted by inverter 96 for generating an e_{2k} even timing signal. The e_{2k} even and e_{2k+1} odd timing error signals are alternately processed and combined by the loop filter 97 to form the $e^{-j\hat{\theta}}$ phase adjustment signal 59. The e_{2k} even and e_{2k+1} odd timing error signals drive a loop filter 97 that in turn controls a VCO 98 that generates the $e^{-j\hat{\theta}}$ phase adjustment signal 59. As may now be apparent, the carrier phase synchronizer 60 is part of a loop between the $e^{-j\hat{\theta}}$ phase adjustment signal 59 and the $r_n e^{-j\hat{\theta}}$ input sampled signal 61 with the loop extending through the isolators 74 and 76, samplers 80 and 82, transformers 86 and 88, hard limiters 90a and 90b, samplers 94a and 94b, mixers 92a and 92b, loop filter 97 and VCO 98 for providing the $e^{-j\hat{\theta}}$ phase adjustment signal 59, while concurrently generating the $\hat{d}_n$ data estimate 15.

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